REMARKS

Applicants have carefully reviewed the Office Action dated October 20, 2006. Applicants have amended Claims 1 and 9 to more clearly point out the present inventive concept. Reconsideration and favorable action is respectfully requested.

The Examiner has objected to the drawings and has required substitute drawings. These have been provided in connection with this response.

Claims 1-8 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and specifically claim the subject matter which Applicants regard as the invention. The Examiner has requested correction and/or clarification.

The Examiner has objected to the term or recitation "a first sampling rate" on line 5, as the Examiner considers this to be indefinite. The Examiner indicates that the first sampling rate could be the "frequency of sampling" or it could be the "time period of time during it [sic] sampling happens." Applicants believe that the language with respect to the sampling rate is clear. A sampling rate is well understood in the industry to be the rate at which samples are taken. For example, if samples were taken at a sampling frequency of 1 Gb, this would mean that each sample were taken at a rate of one sample each nanosecond. This term "sampling rate" does not refer to the amount of time during which the sample is taken, but rather, to the time at which each sample is initiated. Therefore, if samples were taken at a 1 Gb rate, that would mean that the initiation of a sample would be every one nanosecond and the length of time for the sample would be whatever is required for the sample. Thus, to state that an input voltage is sampled "at a first sampling rate" is believed to be very clear and is conventional with respect to industry terminology. These are readily available definitions. For example, one definition of a sampling rate is expressed in "samples per second or hertz (Hz), the rate at which samples of an analog signal are taken in order to be converted into digital form. A PC's sound card typically will sample a received analog signal, such as through a microphone, and digitize it for use by the computer. A higher sampling rate provides a better quality reproduction than a lower sampling rate." (http://www.webopedia.com/term/s/sampling_rate.html) Applicants, if necessary, can provide more detailed documentation and support if the Examiner requires further explanation.

The second term that the Examiner objected to was the use of a "first time" on line 6 and "a second time" on line 8. The Examiner has considered these to be indefinite as they are not clear as to what they mean. Applicants have amended the claim to define these as a first "point' in time. Currently, there are two non overlapping clocks, one for sampling and one for dumping. These are two distinct times and Applicants believe that the amendments to the claims clarify this point. Clearly, in any sampling system, voltage has to be first sampled onto the capacitor and then later dumped from that sampling capacitor onto the feedback capacitor. Applicants believe that no further clarification is required.

The Examiner has also objected to the terminology "dumping charge from the input sampling capacitor to the non-inverting input of the amplifier at a second time and at the first sampling rate" as being indefinite and confusing. For some reason, the Examiner indicates that the clock $Ø_2$ is at a different sampling rate. However, it is clear that $Ø_1$ and $Ø_2$ operate at the same sampling rate, i.e., they both occur at the same rate or same sampling frequency, although they are not overlapping. Applicants do not understand the Examiner's confusion on this point and do not understand what the Examiner means by the assumption that "the rate is the high time period" which is confusing, as the rate is the "rate of occurrence" of the pulses as opposed to the length of time any one pulse is high. If the Examiner needs further clarification, Applicants can provide such.

Further, the Examiner has indicated that the reference voltage and the input voltage are sampled at a different clock rate. This is incorrect and is not disclosed as such. All that is disclosed is that there is a logic state "D" that determines whether V_{REF+} or V_{REF-} is sampled. However, once the "D" state is set, then the sampling operations occurat the correct sampling rate, i.e., the state "D" does not change but, rather, just selects. This is described in paragraph 14 and it is believed to be clear. Applicants believe no further clarification on this point is required.

The Examiner has also objected to the recitation "a first sampling rate" on line 10 as not being clear as to whether it is the same or different than the "first sampling rate" in line 5. However, the claim sets forth that the sampling rate is the same and the specification supports such, since, when the state "D" is in a particular state, the same reference voltage is always sampled at the rate of $Ø_1$.

The Examiner has objected to the term "a second sampling rate" on line 12 as unclear. However, it can be seen that the charge is dumped onto the input of the amplifier under control of the clock signal $Ø_a.Ø_2$ and this clearly occurs at a different rate than either $Ø_1$ or $Ø_2$. Since $Ø_2$ dumps charge from the input sampling capacitor and $Ø_a.Ø_2$ dumps charge from the feedback sampling capacitor, it can be seen that, for example, in Fig. 2, that the rate is at least one half that of $Ø_2$. Thus, there is clearly described a second sampling rate that is different than the first sampling rate. Applicants believe no further clarification is required on this point.

The Examiner indicates that the terminology "controlling the amount of time the charge is dumped from the feedback sampling capacitor to be substantially equal to the amount of time the charge is being dumped from the input sampling capacitor" is indefinite because it is mis-descriptive. The Examiner indicates that Fig. 1 shows that "charge is dumped from the feedback sampling capacitor" with the clock $Ø_2.Ø_a$ and that the "charge is dumped from the input sampling capacitor" with clock $Ø_2$. Clearly, this is the case. However, the Examiner indicates that these clocks are not similar. Applicants refer the Examiner to paragraph 17 wherein it states that "Therefore, with the embodiment illustrated above, and ensuring that the time between the rising edge 220 and falling edge 22 of the wave form $Ø_a.Ø_2$ is substantially equal to the length of pulse $Ø_2$ beginning at leading edge 216, this will ensure that they are relatively well balanced." This language clearly shows that the pulse width between edges 220 and 222 is substantially equal to the pulse width of the pulse beginning at edge 316. Thus, Applicants believe that the specification clearly supports this terminology and Applicants believe that no further clarification is required.

In view of the above, Applicant respectfully requests withdrawal of the 35 U.S.C. § 112 with respect to claims 1-8.

Claims 1-16 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Shin* (U.S. Patent No. 6,107,871). This rejection is respectfully traversed with respect to the claims as currently presented.

The Examiner has specifically stated that, regarding Claim 1 and Figs. 6, 7 and 8 of *Shin*, there is shown a method for driving the input of the integrator in a delta-sigma converter and

further that it includes a step of "wherein varying the 'second sampling rate' (Ø2) relative to the 'first sampling rate' change [sic] the gain of a delta-sigma converter." Applicants disagree with this argument in that there is no disclosure in *Shin* of the ability to change any clock rates relative to the other. Applicants believe that the lack of disclosure or any suggestion of changing clock rates to change the gain in *Shin* renders this reference a non-obviating and non-anticipatory reference. Therefore, Applicants respectfully request withdrawal of the 35 U.S.C. § 102 rejection with respect to Claims 1-16 in view of *Shin*.

Applicants have now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicants respectfully request full allowance of the claims as amended. Please charge any additional fees or deficiencies in fees or credit any overpayment to Deposit Account No. 20-0780/CYGL-26,655 of HOWISON & ARNOTT, L.L.P.

Respectfully submitted,
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